IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/780,377

First Named Inventor: Youval Nehmadi

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Art unit: 2822
Examiner: Picardat, Kevin M.

Docket No.: PDC/MDR/8317

Confirmation No.: 1805

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450.

**DECLARATION OF YOUVAL NEHMADI**

Yoval Nehmadi declares:

1. I am a co-inventor of the above-captioned patent application. I have personal knowledge of the facts set forth herein except where such information is stated to be upon information and belief, in which cases I believe such information to be true.

2. I understand that claims 1-25 of this application have been rejected as being anticipated by Volk et al., US Patent application Publication 2005/0004774, which has an earliest effective filing date of 3 July 2003.

3. The presently claimed invention was conceived prior to 3 July 2003. Attached hereto as Exhibit A is a copy of an Applied Materials Invention Alert form that I prepared prior to 3 July 2003. The Invention Alert includes as an attachment a document entitled "CAD info in DMS and other application", which I prepared and which describes the presently claimed invention. Portions of the Invention Alert and its attachments have been redacted.

4. Subsequent to submitting the Invention Alert, and prior to 3 July 2003, I prepared a second document entitled "CAD info in PDC tools". A copy of this document (redacted) is attached hereto as Exhibit B. This document further describes the presently claimed invention.

5. Following submission of the second document, Exhibit B, I worked quickly to have the provisional application 60/486,565 on which the present application is based prepared and filed. The provisional application was filed 11 July 2003, and included the relevant portions of Exhibits A and B.

6. All of the activities described herein took place in Israel and the United States.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct and understand that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Dated: _____

_____
Yoval Nehmadi

4. Subsequent to submitting the Invention Alert, and prior to 3 July 2003, I prepared a second document entitled "CAD info in PDC tools". A copy of this document (redacted) is attached hereto as Exhibit B. This document further describes the presently claimed invention.

5. Following submission of the second document, Exhibit B, I worked quickly to have the provisional application 60/486,565 on which the present application is based prepared and filed. The provisional application was filed 11 July 2003, and included the relevant portions of Exhibits A and B.

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Dated: 5/31/06

Yoval Nehmadi

**Exhibit A to DECLARATION OF YOUVAL NEHMADI**

86

# INVENTION ALERT FORM

**TO: Gaile Bailey M/S 2061/Extension 32724**
**Date:** [redacted] COMPUTER ENTERED 0008317

**CIRCLE ONLY ONE FROM TOP ROW(REQUIRED FIELD):-** [redacted]

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EPI/ SUBSTRATE 2470 | CMP 1399 | METAL 0881 | CPS 0676 | CORE ENG 0793 | COPPER 2492 | AKT | ATD 1301 | APD | FET 3037 | HDPCVD 0281 | |
| SPC 2512 | | SILICON 0916 | SMO/ GAS 1649 | EPS 2590 | ALUMINUM 2492 | EBT | | CDSEM | MDR/ DSI 3047 | BCVD 0166 | |
| TPG/RTP 0584 | | DIELECTRIC/ RIE 0521 | SMO/ PUMP 1651 | DT 2492 | LINER/ BARRIER 2492 | | | NBD | | LOW K 2445 | |
| TPG/LPVD 0584 | | DIELECTRIC/ ICP 0521 | EPIC 2442 | | | | | DRSEM | | ELK 2445 | |
| TPG/GATE 0584 | | CONDUCTOR 0894 | SCALPEL | | | | | ISW | | | |
| TPG/OTHER 0584 | | CHAMBER TECH 0894 | CONSILIUM 2199 | | | | | ICT | | | |
| PMD 3002 | | CORE TECH 1245 | | | | | | EBI | | | |
| | | | | | | | | Oramir | | | |
| STI | | | | | COPPER | | | | | Dual Dam | |
| CAP | | | | | | | | | | | |
| GATE STACK-1498 | | | | | | | | | | | |

1. Title of Invention (please print clearly): **CAD information in DMS and other application**

2. Inventors-Names only-(please print clearly and provide complete information at Section 9.)

**Youval Nehmadi**

Please use separate attachments for any answers that don't fit on the form, especially for questions 3-8. If the answer to a question is "NONE", please write "NONE" rather than leaving the answer blank.

3. Earliest dates and model names of all Applied products incorporating the invention which have been offered for sale or are expected to be offered for sale:

**TRIX and PDC inspection and revue tools**

[redacted]

4. If the invention has been demonstrated or described to persons other than Applied employees, for each disclosure please provide the earliest date, name of company, a brief description of what was disclosed and the purpose of the disclosure. Attach a copy of any related non-disclosure agreements:

no

5. If future disclosures like those in Question #4 are expected to occur within the next 12 months, please provide the anticipated date, type of information to be disclosed, and purpose of the disclosure:

[redacted]

6. Describe any other known designs or processes, whether actually implemented or merely proposed in a publication, which could be considered similar to your invention or which constitute the state-of-the-art improved upon by your invention: If described in a publication, attach a copy of same or provide a citation.

7. List each feature of the invention which you consider novel and non-obvious. Describe the advantages of each novel feature in comparison with the state-of-the-art approaches which are most similar to your invention:

**This document describes some ideas related to:**
**Using of CAD information in DMS system and in PDC tools**
**SEM electrical failures (open\short) detection**
**Real vision for real wafers**
**____see attached documents**

8. Describe the invention, preferably with reference to attached drawings:

**____see attached documents**

Provide the following information for **EACH** inventor** REQUIRED FIELDS:

**Inventor #1:**
Legal Name: Employee # **74912_** Mail Stop_5800
Work Phone Fax No.: **_(972)-8-9488283**
Job Title: **algorithm manager** GM PDC
Citizenship: **Isreal**
Complete Home Address **Nili (D.N. modin) 71930**
Manager: **Ariel Ben-Porath** Title: **KPU manager**
Div. Manager **Ofer Bokobza** Title: _
Product Group: Cost Center #:

**Inventor #2:**
Legal Name: Employee # _____ Mail Stop 5800
Work Phone _____ Fax No.: _____
Job Title: _____
Citizenship: _____ IL_____
Home Address: _____
Manager: _____ Title: _____
Div. Manager _____ Title: _____
Product Group: _____ Dept #: _____

10. Signature, date and **PRINTED** name of each inventor plus two witnesses who have read and understood this Invention Alert form:

**Inventors**: YOUVAL NEHMADI [redacted] _____

| Printed Name | Date | Signature |
|---|---|---|
| | | |
| Printed Name | Date | Signature |
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|---|---|---|
| 4. | | |
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| Printed Name | Date | Signature |
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| | | |

**Witness:**

| Printed Name | Date | Signature |
|---|---|---|
| YOSSI REZCH | [redacted] | |
| ARIEL BEN-PORATH | [redacted] | A. Ben-Porath |

**Return to:** **Gaile Bailey**
**Mail Stop:** **2061**
**Fax No.:.:** **986-3090**
**Extension:** **563-2724**

**PDC**
**PSW KPU**

APPLIED MATERIALS®

# *CAD info in DMS and other application*

**Revision**: 1.0 *Draft*
**Date:** [redacted]
**Author**: Youval Nehmadi

# Table of Contents

# 1 General

## 1.1 Preface

This document describes some ideas related to:

- Using of CAD information in DMS
- SEM electrical failures (open\short) detection
- RealVision for real wafers (Production wafers)

## 1.2 References

[1] DSI

## 1.3 Terms and abbreviations

| | |
|---|---|
| ADC | - Automatic Defect Classification, done by SEM Vision during wafer review |
| ADR | - Automatic Defect Review, done by SEM Vision during wafer review |
| API | - Automatic process inspection |
| Compass | - Wafer inspection tool, developed in PDC |
| SEM Vision | - Automatic Defect Review tool, developed in PDC |
| YMS | - Yield Management System |
| DMS | - Defect Management System |
| E-test | - Electrical Tests |
| CAD | - Computer added design |

## 1.4 Revision History

| *Version* | *Date* | *Description* |
|---|---|---|
| 1 | [redacted] | Youval Nehamdi |

# 2 Introduction

TBD

# 3 Inspection tools

## 3.1 Auto select notch direction

Selecting automatically the best notch (Up/Down/Left/Right) direction for inspection can be done using CAD information. Using the CAD info we can calculate the conducting lines' directions and the die length and width. By knowing the direction of the lines and the die length and width we can calculate best notch direction for inspection on the Compass. The notch direction is a compromise between two variables:

- Lines direction: In order to minimize saturation we would like to insert the wafer so that most of the lines in the wafer will be parallel to the laser beam scanning direction.
- Die length and width: To achieve the best throughput it is better to insert the wafer so that the long size of the die will be parallel to the laser beam scanning direction.

## 3.2 Auto CLC mask

### 3.2.1 Automatic tuning CLC mask

The CLC mask increases the detector sensitivity by masking the constructed interference locations. The constructed interference is built by the reflection of repetitive patterns (lines, via, etc.) located on the wafer. Using the CAD the main wafer frequencies (generated by the wafer lines, via, etc.) are calculated. Knowing the wafer frequencies we calculate the constructed interference locations. Those locations are the regions that should be blocked by the CLC mask.

### 3.2.2 New CLC scanning strategy

Automatic analysis of the CLC using the CAD may define a new scanning strategy, a scanning with different CLC masks for the different wafer/die regions (logic, bare, memory, periphery etc.). Using for each region the appropriate CLC mask (can be done by inspecting the wafer few times each time for a different region) will increase the sensitivity of the detectors.

## 3.3 Auto define different regions

### 3.3.1 Automatic tuning regions

Different regions (logic, bare, memory, periphery etc.) in the wafer reflect the light differently. As a result of that the inspection sensitivity (beam energy, detectors sensitivity, etc.) should be different for different regions. Using the CAD information we can automatically define different regions and eliminate this step from the inspection tools tuning procedure.

### 3.3.2 New scanning strategy

Automatic analysis of the different regions using the CAD may define a new scanning strategy, a scanning with more than two different regions. Using for each region appropriate imaging characteristic (beam energy, detectors sensitivity, etc.) will increase the sensitivity.

## 3.4 Classification

The CAD can help in making classification in the Compass.

Enhance OTF classification
Combining the detectors data with the pattern direction around the defect will change the classification procedure and will increase the accuracy of the OTF classification. Examples:

- Knowing the pattern direction and the increase of intensity in certain detectors can be taken into account.
- Knowing that the defect is located near a pattern increases its likelihood to be a pattern defect.
- Knowing that the defect is located in a bare region decreases its likelihood to be a pattern defect.

Find Killer defects
Using the CAD and the defect location we can detect killer defects. Knowing defect characteristics (size, location, etc.) and the pattern characteristic (density, width, etc.) we can estimate the defect's likelihood to make shorts/opens and detect killer defects.
Example:
A memory die is separated into periphery and memory cells zones. In the memory cells zone there is a redundancy, so defects which connect two lines will not necessary be killers; while in the periphery each defect that connect/disconnect a line is a killer. Using the CAD we can:

- Know whether the defect lies in the periphery or not
- Estimate (using also the defect size, intensity, etc.) the defect's likelihood to make shorts/opens.

By using the above and other defect and pattern characteristic we can detect killer defects.

Labeling according to regions
Defect region labeling according to the defect's (logic, bare, memory, periphery etc.) location can be done using the CAD information. This enables better sampling for review and enhances the correlations, etc.

## 3.5 Global Alignment

- Automatically define Global Alignment targets by CAD.

## 3.6 Other

- Analysis that will define which Compass recipe to use. Analyzing the CAD we can indicate the recipe type (predefine recipe).
- Define scanning strategy.
- Knowing the CAD info can eliminate regions that are not important.

# 4 SEM

## 4.1 SEM Electrical failures (open\short) detection

### 4.1.1 Short/open on very large regions

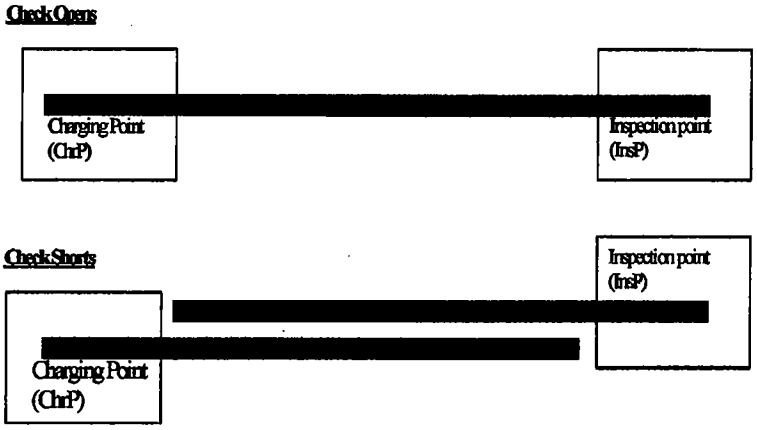
This application can detect electrical failures (lines short/open) on very large regions (it may be applicable for memory even without CAD information).

Using the CAD information we can create a smart recipe for failure analysis using SEM voltage contrast capabilities. This recipe will define:

- Charging points (ChrP): regions in which we charge the pattern.
- Inspection points (InsP): regions that should be inspected in order find if there was a short/open.

The inspection will be done by charging in a certain location (ChrP) and do inspection on another location (InsP) that is far from the charged one. According to the CAD we can know if the inspection regions should be charged or not. Using the InsP and ChrP we will be able to detect:

- Open: If the InsP and ChrP are connected by pattern we expect that by charging the ChrP the InsP will be also charged. If the InsP is not charged there is an open. The open analysis can be done when the InsP and ChrP are far from each other to enable large area inspection.
- Short: If the InsP and ChrP are not connected by pattern we expect that by charging the ChrP the InsP will not be charged. If the InsP is charged there is a short between InsP and ChrP. The short analysis by definition detects all possible regions for short between InsP and ChrP. To enable large area inspection we should locate InsP and ChrP that have a large area that can have a short.




### 4.1.2 T Scan for real wafer

T Scan for real wafer – Using the CAD to plan T Scan test for real wafer.

## 4.2 Non-reference ADR

By using the CAD information a "reference image" can be produced. The ADR (ADR that will be based on edges) can use this image to make a non-reference ADR. Non-reference ADR will provide better SEM Vision throughput (approximately 150% faster).

### 4.3 Automatically create API recipe

Automatically create recipe for API by analyzing the CAD and discovering regions that are in higher likelihood to be defected (end of lines, close via, small via, line close to border, line close to line, etc.) or regions where a defect is likely to be killer (the periphery region in memory, very dense regions in logic, etc.). Those regions are automatically selected to be in an API recipe.

### 4.4 Defect sampling

Different regions (logic, bare, memory, periphery etc.) in the die have different levels of significance depending on the role they have (example: the periphery in memory dies is more important than the memory itself since the memory has redundancy and the periphery not). Different regions also vary in their probability to have shorts or opens (example: dense regions are more likely to have short). Because of the above it is important to sample according to the defect location region.

Using the CAD enable us to sample according to a region on the die.

### 4.5 Other

#### 4.5.1 Segmentation auto tuning

Eliminate the segmentation step in ADC tuning procedure using CAD information.

#### 4.5.2 Classification

Can help in ADC.

#### 4.5.3 E-test failure to API recipe

See: DMS, Find the E-test failures location, chapter 7.4, page 8

## 5 CD

### 5.1 Automatically create CD recipe

## 6 RealVision

### 6.1 Mask auto analysis for the real vision

Analyzing the CAD files we can calculate the process characteristic (via space, via width line pitch, line width, etc.), statistics of the product to be produced. Using the process characteristic statistic we can automatically design DOE (Design of Experiment) and give the output CAD information for the mask and the parameters for real vision and the tester.

### 6.2 Real vision for real wafers

Connect a real die on certain lines to pads and use the tester to check the die, when the wafer is cut those connections will be isolated. The CAD information will be used in order to know which E-test to make (it can be done also without CAD).

# 7 DMS

## 7.1 View CAD with images

### 7.1.1 On TRIX

See the CAD info combined with defect images in the DSI view. This can be done for SEM images, optic images, defect maps, Bitmaps, Binmap, etc.

### 7.1.2 On other tools

Enable to see CAD information combined with defect images on other tools (SEM Vision and Compass, etc.). This can be done by getting the image location, creating a CAD map around this location, and sending it to the tool.

## 7.2 Defect sampling

See: SEM, Defect sampling, 1chapter 4.4, page 7.

## 7.3 Classification and killer defect detection

### 7.3.1 Enhance classification

Use Compass SEM CAD results to provide better classification.

### 7.3.2 Killer defect detection

Different regions (logic, bare, memory, periphery etc.) in the die have different tendencies to be killers depending on the role they have (example: defects in the periphery in memory dies have higher likelihood to be killers than the memory itself since the memory has redundancy and the periphery not). Different regions also vary in their probability to have shorts or opens (example: dense regions are more likely to have short).

Killer detection analysis will calculate the defect's likelihood to be a killer by using the defect's size and other parameters and as well the location on the CAD files.

## 7.4 Find the E-test failures location

### 7.4.1 Correlate defect with E-test failures

Knowing the electrical test failure we can find the defect's location (along a line or in a certain point) using CAD information (We can do it also for logic). This enables us to correlate electrical tests (Binmap, Bitmaps) to inspection results. This can help to find the defect causing the electrical failure.

### 7.4.2 Auto create API recipe from E-test failures

This application can be used in order to build automatically an API recipe that will inspect the region causing the electrical failures. This recipe can be used during a period when this specific electrical failure happens.

## 7.5 Other

- Predict yield knowing the inspection results and the location on the die (if the defects are in a dense area it is more likely that the defect is a killer).
- Yield prediction by using correlation between E-test, Defect density, CAD, ADC Classification OTF, etc.

Gaila Bailey

Please e-male me when you got this invention alert
Youval_nehmadi@amat.com

Thanks
Youval Nehmadi

**Exhibit B to DECLARATION OF YOUVAL NEHMADI**

**PDC**
**PSW KPU**

APPLIED MATERIALS®

# *CAD info in PDC tools*

**Revision:** 1.0 ***Draft***
**Date:** [redacted]
**Author:** Youval Nehmadi

# Table of Contents

# 1 General

## 1.1 Preface

## 1.2 References

[1] DSI

## 1.3 Terms and abbreviations

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| ADR | - Automatic Defect Review, done by SEM Vision during wafer review |
| API | - Automatic Process Inspection |
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| SEM Vision | - Automatic Defect Review tool, developed in PDC |
| YMS | - Yield Management System |
| DMS | - Defect Management System |
| E-test | - Electrical tests |
| CAD | - Computer added design |

## 1.4 Revision History

| *Version* | *Date* | *Description* |
|---|---|---|
| 1 | [redacted] | Youval Nehmadi |

# 2 Introduction

This document describes applications using CAD information for the benefit of the PDC tools. This document is built according to the different PDC tools. The applications in each tool ~~each~~ are listed according to their priority.

For certain regions on the chip it is very important that they will be matched (for example: matched transistors in differential amplifiers). Using the design information we can locate those regions and make an application that will check whether the regions on the wafer are matching.

# 5 SEM

## 5.1 Charge & view application

### 5.1.1 Short/open on very large regions

It is a charge and view application (see Appendix) that is based on SEM Vision's voltage contrast capabilities. Using CAD information the "natural test structures" (regions that can be inspected by charge and view application, for example: parallel metal and poly line in memory, bus in logic) are detected and a recipe specifying the charging point and the view points is defined. This recipe is able to run on the SEM Vision and to detect short/open on very large regions in a short time.
In the new technology large regions in the die can be defined as "natural test structures" (for example: 128 bus and memory). Using this application those regions can be inspected for short/open failures in a very fast and effective way.

## 5.2 Automatically create API recipe

Automatically create recipe for API by analyzing the CAD and discovering regions that are in higher likelihood to be defected (end of lines, close via, small via, line close to border, line close to line, etc.) or regions where a defect is likely to be killer (the periphery region in memory, very dense regions in logic, etc.). Those regions are automatically selected to be in an API recipe.

## 5.3 Define regions for Cell2Cell (or image 2 online image database)

Define automatically regions that are applicable to SEM Vision's Cell2cell application. Those regions will be defined according to their maximum repetitive period length. The maximum repetitive period length should define the field of view that the reference images should cover. Later each defect image would be compared to those reference images.

## 5.4 Specimen current

A specimen current is an important measurement that can be done on the SEM Vision (or in stand alone tools). One of the major problems in this application is that it is difficult to know what is the expected specimen current. Using the CAD information we can know in advance the expected specimen current.

Using the CAD information the recipe can be created automatically. This recipe will define the proper location for measurement and the required current. Such a recipe will be localizing the most important measurements' sights by using predefined knowledge and the 3D wafer structure.

## 5.5 Additional

- Segmentation auto tuning - Eliminate the segmentation step in ADC tuning procedure using CAD information.
- Classification - Can help in ADC.
- Non-reference ADR - By using the CAD information a "reference image" can be produced. The ADR (ADR that will be based on edges) can use this image to make a non-reference ADR. Non-reference ADR will provide better SEM Vision throughput (approximately 150% faster).

# 6 RT

## 6.1 RT sites by layout & design

This application selects the RT sites using a combination of layout (e.g. dense area) and design (e.g. critical path for device timing).

### 6.1.1 Metrology

Pre-define set of measurement sites, base on pre-defined rules. Examples are High-MEEF locations, Critical features where critical might be defined as **performance-based** cases (for example: location that is critical for the transistor timing) or **manufacturing-base** cases (for example: location that is susceptible for CD problem).

### 6.1.2 Inspection

Pre-defined locations/areas that will serve as an input for the following sub-applications:

- Full plate uniformity mapping (LBM style but concentrate on critical features)
- Less/More critical regions that should be treated differently either at inspection time and/or later at post processing time
- Fab application - set of locations that can serve as a base for a PWT (Process Window Trends) tool.

## 6.2 RT Match verification

For certain regions on the chip it is very important that they will be matched (for example: matched transistors in differential amplifiers). Using the design information we can locate those regions and make an application that will check whether the regions on the wafer are matching.

# 7 TRIX

## 7.1 View CAD with images

### 7.1.1 On TRIX

See the CAD info combined with defect images in the DSI view. This can be done for SEM images, optic images, defect maps, Bitmaps, Binmap, etc.

### 7.1.2 On other tools

It enables viewing CAD information combined with defect images on other tools (SEM Vision and Inspection tool, etc.). This can be done by getting the image location, creating a CAD map around this location, and sending it to the tool.

## 7.2 Classification and killer defect detection

### 7.2.1 Enhance classification

Use Inspection tool SEM CAD results to provide better classification.

### 7.2.2 Killer defect detection

Different regions (logic, bare, memory, periphery etc.) in the die have different levels of significance and different tendencies to be killers depending on the role they have (for example: defects in the periphery in memory dies have higher likelihood to be killers than the memory itself since the memory has redundancy and the periphery not). Different regions also vary in their probability to have shorts or opens (for example: dense regions are more likely to have shorts).

Killer detection analysis will calculate the defect's likelihood to be a killer by using the defect's size the location on the CAD files and as well other parameters.

### 7.2.3 Defect sampling

From the same reasoning as mention above (in killer defect detection) it is important to sample according to the defect location zone.

### 7.3 Find the E-test failures location

#### 7.3.1 Correlate defect with E-test failures

Knowing the electrical test failure we can find the defect's location (along a line or in a certain point) using CAD information (we can do it also for logic). This enables us to correlate electrical tests (Binmap, Bitmaps) to inspection results. This can help to find the defect causing the electrical failure.

#### 7.3.2 Auto create API recipe from E-test failures

This application can be used in order to build automatically an API recipe that will inspect the region causing the electrical failures. This recipe can be used during a period when this specific electrical failure happens.

### 7.4 Additional

- Predict yield knowing the inspection results and the location on the die (if the defects are in a dense area it is more likely that the defect is a killer).
- Yield prediction by using correlation between E-test, defect density, CAD, ADC Classification, OTF, etc.

## 8 Process tools

### 8.1 Selecting Etch recipe

Reticle transmission data is the percent chrome on the reticle. This affects the amount of residual resist that is left on the wafer. The amount of resist on the wafer has a small but measurable impact on photo CDs. This contribution could be modeled by feed-forward CD algorithms. The amount of resist on the wafer also has a small but measurable impact on etch operations. For high transmission reticles, the loading in the etch is higher and this can lead to problems. We continually run into incomplete etch at pad mask, the etch for the top layer passivation, due to high transmission reticles on small chips. This has lead to wafer scrap at the last process step. The problem was bad enough for us to develop a manual solution.

There are already sources of reticle transmission data, so this is not a new approach. Stepper/scanners can read the reticle transmission. What may be missing is a way of systematically using this information. We used a manual system of assigning a different etch recipe. A short, regular or long etch recipe was used for the low, regular of high transission reticles for pad mask etch. We wanted to apply this to gate CD control as well but etch was reluctant to write the software or to have too many manual systems in place. If DBM managed this it may be a small contribution to the total package.

## 9 Real Vision

### 9.1 Mask auto analysis for the real vision

Analyzing the CAD files we can calculate the process characteristics (via space, via width line pitch, line width, etc.), statistics of the product to be produced. Using the process characteristic statistics we can automatically design DOE (Design of Experiment) and give the output CAD information for the mask and the parameters for Real Vision and the tester.

### 9.2 Real Vision for real wafers

Connect a real die on certain lines to pads and use the tester to check the die, when the wafer is cut those connections will be isolated. The CAD information will be used in order to know which E-test to make (it can be done also without CAD).

# 10 Appendix A: SEM Electrical failures (open\short) detection

## 10.1 Short/open on very large regions

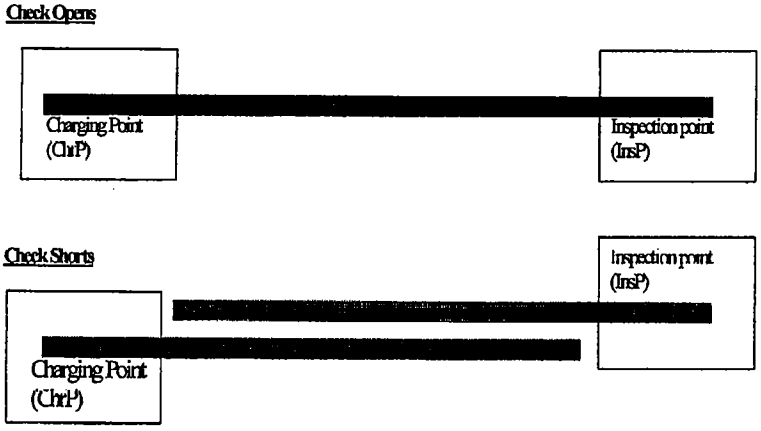
This application can detect electrical failures (lines short/open) on very large regions (it may be applicable for memory even without CAD information).

Using the CAD information we can create a smart recipe for failure analysis using SEM voltage contrast capabilities. This recipe will define:

- Charging points (ChrP): regions in which we charge the pattern.
- Inspection points (InsP): regions that should be inspected in order find if there was a short/open.

The inspection will be done by charging in a certain location (ChrP) and doing inspection on another location (InsP) that is far from the charged one. According to the CAD we can know if the inspection regions should be charged or not. Using the InsP and ChrP we will be able to detect:

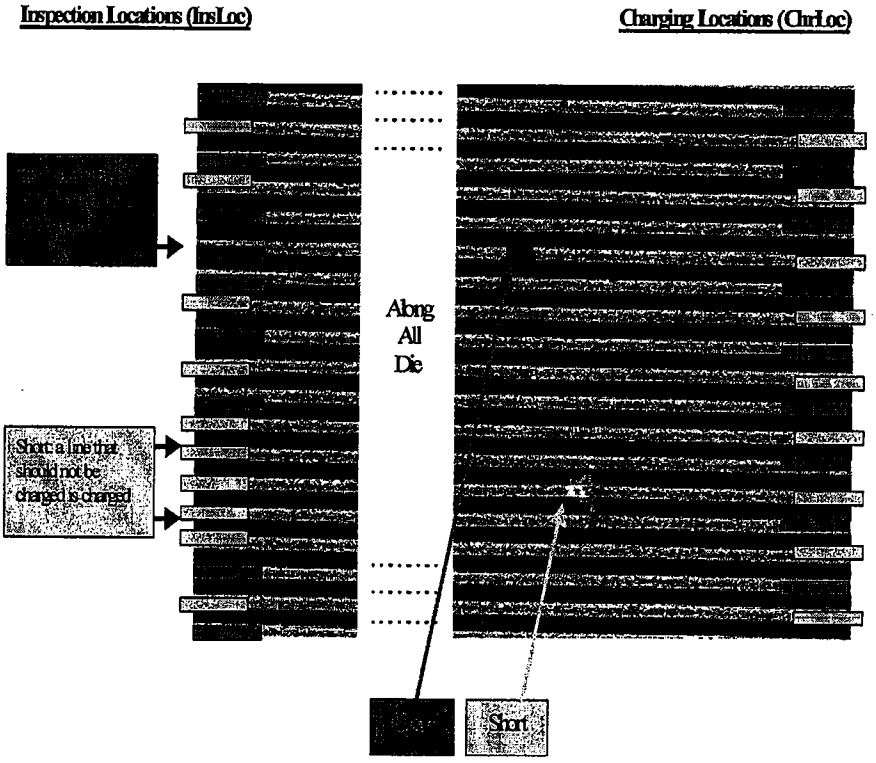
- Open: If the InsP and ChrP are connected by pattern we expect that by charging the ChrP the InsP will be also charged. If the InsP is not charged there is an open. The open analysis can be done when the InsP and ChrP are far from each other to enable large area inspection.
- Short: If the InsP and ChrP are not connected by pattern we expect that by charging the ChrP the InsP will not be charged. If the InsP is charged there is a short between InsP and ChrP. The short analysis by definition detects all possible regions for short between InsP and ChrP. To enable large area inspection we should locate InsP and ChrP that have a large area where a short may appear.




To illustrate the application "SEM Electrical failures (open\short) detection" the API recipe for M1 recipe in memory can look as follows (See Figure 2):

1. Go to the die's right side
2. Charge each second line
3. Go to the die's left side
4. Check that every second line is charged. If not keep the suspected short/open location (the defect location should be along the metal line)
5. Repeat 1-4 until all the die is scanned

6. Go to each suspected short/open location, scan along the metal line and find the defect causing the short/open.




### 10.1.1 T Scan for real wafer

T Scan for real wafer – Using the CAD to plan T Scan test for real wafer.

Inventors

| | |
|---|---|
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| Josephine Phua | 1656 Pala Ranch Circle. San Jose. CA 95133 USA. |
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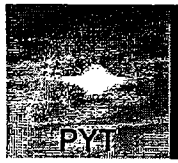
| | Application | Value | Remarks |
|---|---|---|---|
| 1 | Select inspection & measurement sites for CD tools, E-beam inspection tools, optical inspection tools, process monitoring tools such as API on SEMVision.<br><br>Use the CAD in order to automatically or manually select on the wafer or on the mask the locations that are more susceptible to problems. The list of sites will be transfer to the tools for inspection review or monitoring. | Improve resulting sensitivity in critical locations & areas.<br>Reduce overall recipe setup time.<br>Increase return on investment on metrology and inspection machines.<br>Improve machine utilization.<br>Allow tighter control limits when monitoring various process variables.<br>Enable reaching of higher yields, improving revenue.<br>Provide feedback to designers on the manufacturability of specific devices as they designate. | Examples:<br>Sites susceptible to systematic process problems<br>Sites critical to chip functionality, reliability or performance (e.g. clock rating)<br>Matched transistors in operational amps or push-pull stages or elsewhere<br>Critical path driver transistors (clock, bus)<br>Non-redundant areas and devices in memory chips<br>Extremely dense or extremely isolated features<br>Critical alignment structures (e.g. self aligned contacts)<br>High MEEF locations<br>OPC on specific spatial arrangement of geometrical objects |
| | Select e-beam inspection regions | Improve return on investment on EBI tools by setting up recipes that cover a sample of each region type, possibly prioritized by criticality, redundancy etc.<br>Provide higher wafer throughput for EBI tools | Use the CAD in order to automatically or manually select on the wafer or on the mask the regions that are more susceptible to problems. The list of regions will be transfer to the tools for inspection or/and review and/or monitoring. |

| | | | |
|---|---|---|---|
| 2 | Segment the die according to periodic, random areas and other characteristics, extract period, direction and other characteristics | Simplified optical inspection tuning, Optimize optica inspection multi-tuning, Optimize CLC | Use the CAD in order to automatically and/or manually segment the wafer or musk to regions. Those regions will be used to simplified the inspection tools tuning |
| 3 | Segment the die according to C2C period | SV TPT (C2C areas, die to database), maybe EBI TPT as well | Use the CAD in order to automatically and/or manually segment the wafer or mask to regions that have the same periodicity. Those regions will be used to enable automatically creation of recipe for cell to cell (or golden image) applications |
| 4 | Die to Database defect detection | Detect defects which affect the whole wafer | Use the CAD in order to build a die to database comparison for wafers or masks |
| 5 | Product Information | Automatic generation of die sizes, selection of alignment targets | Generate and send to the tools alignment targets (locations and images generated from the CAD) and product information (the location and sizes of the die and field) |
| "5.<br>5 | Region Criticality, Use in: defect OTF, ADC | | Use the CAD in order segment the wafer or mask to regions that have the same criticality (Criticality - describes the likelihood of different defects sizes to connect the features located on the wafer or mask). |
| 6 | Killer Defect Identification | Assign killer index to each defect based on functional effect on chip | |
| 7 | Defect labeling and sampling for Review | Sample review defect according to region on chip | |
| 8 | Enhance OTF classification | It will increase the OTF accuracy | Combining the detectors' data with the pattern direction around the defect will change the classification procedure |
| 9 | Identify embedded test structures | Use long periodic structures (e.g. word lines, data buses) as built-in test structures for shorts/opens | |

| | | | |
|---|---|---|---|
| 10 | Using design information to select Automatically **Process** tool recipe | Save time in creating and selecting the recipe. Min. mistake in recipe | Examples:<br>Reticle transmission data for Etch recipe selection<br>CMP process selection using layer densities<br>Etch recipe selection using layer densities |
| 11 | Auto select scanning direction | Save time in creating recipe. Enable to build better recipe | Selecting automatically the best notch (Up/Down/Left/Right) direction for inspection, it can be done using CAD information |
| 12 | Find sights for Specimen Current measurement | Using the CAD a recipe can be created automatically with the proper location for measurement and the required current | Such a recipe will be localizing the most important measurement sights by using predefined knowledge and the 3D wafer structure |
| 13 | Segmentation auto tuning | Eliminate the segmentation step in ADC tuning procedure using CAD information | |
| 14 | CAD to Predict yield | Yield prediction | Predict yield knowing the inspection results and the location on the die |
| 15 | CAD auto analysis for DOE test structures | Automatically from the product CAD generate the output CAD information for a DOE test structure mask and the parameters for the tester | Using the process characteristic statistics we can automatically design DOE (Design of Experiment) |
| 16 | DOE on product wafer | Monitor a product die by connecting a product die on certain lines to pads and use the tester to check the die | When the wafer is cut those connections will be isolated |




# Design Based Monitoring


- Overview: Design Based Monitoring
- Applied Materials Approach
- Next Steps / Discussion

**Problem Statement:**

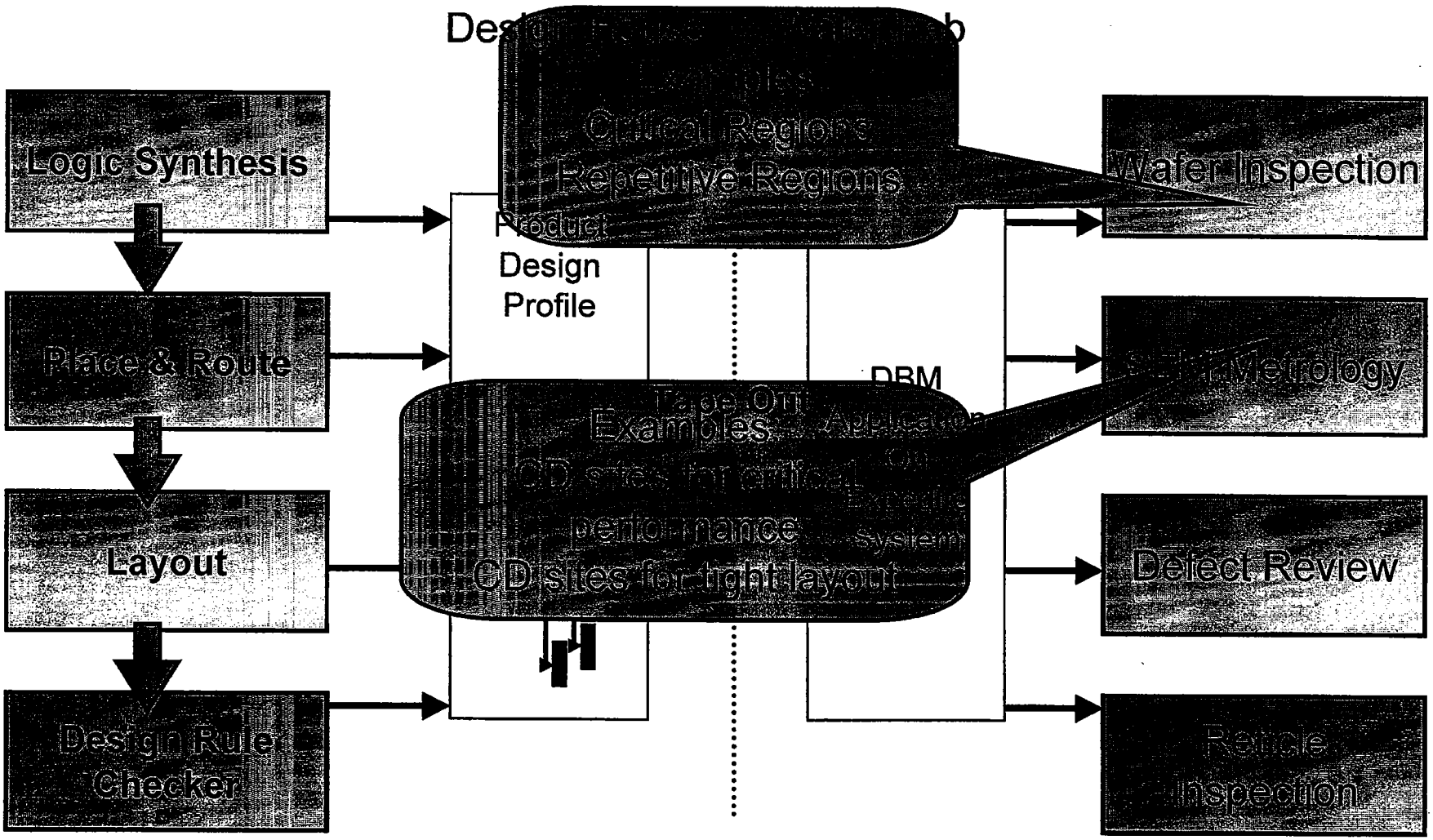
- Limited design information flows to fab floor, hindering the fab process & tool monitoring efficiency

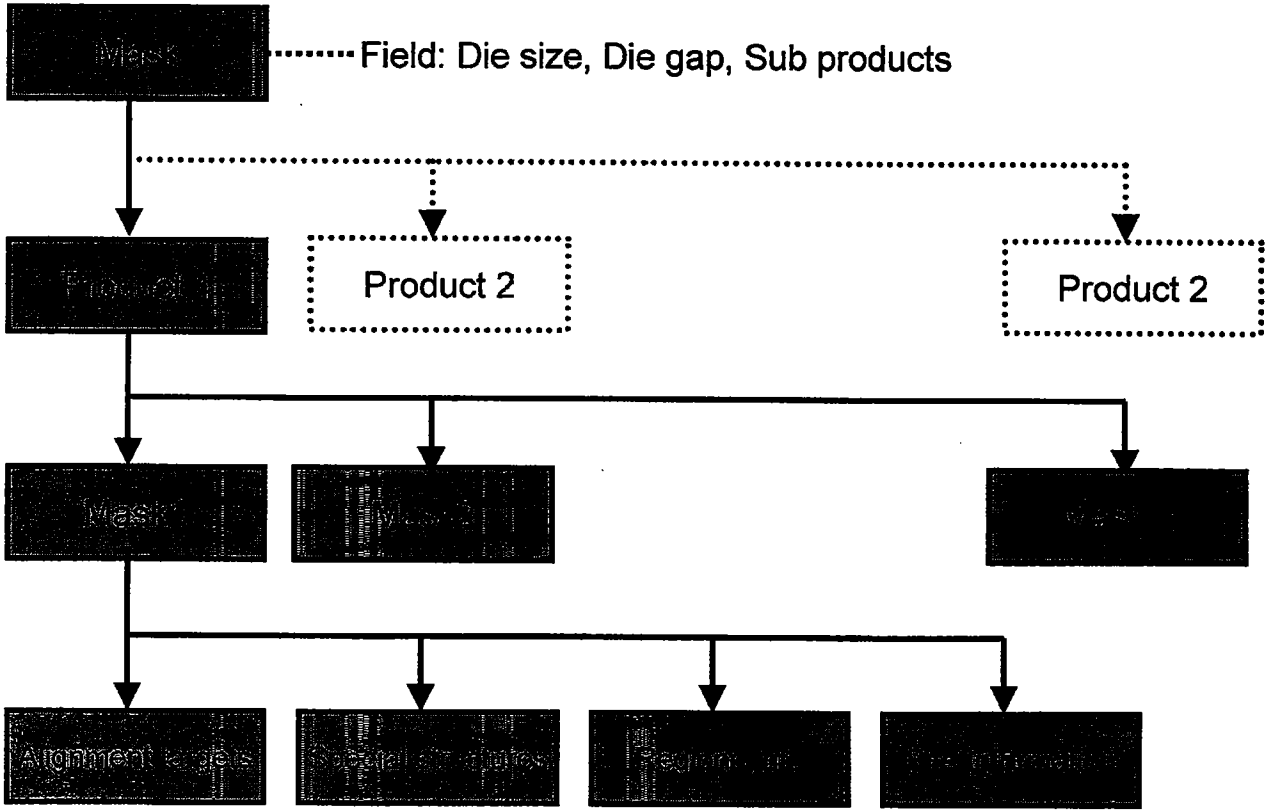
**Solution:**

- Provide a gateway from design tools to the fab, allowing efficient and proactive monitoring capability on PDC tools

**Strategy**:

- Define an open standard that allows EDA tools to extract and save design information
- Define the tools for attaching the design information per product and transferring procedure to the fab
- Provide a gateway application on AMAT's Expedite platform
  - Read incoming design profile, convert to M&I equipment notation and maintain in a database
  - Enable interactive data browsing and navigation
  - Dispatch recipe elements to M&I equipment


Logic Synthesis
Place & Route
Layout
Design Rule Checker
Product Design Profile
Critical Regions
Repetitive Regions
Tape Out Examples
CD sites for critical performance
CD sites for tight layout
DBM
Wafer Inspection
Metrology
Defect Review
Reticle Inspection

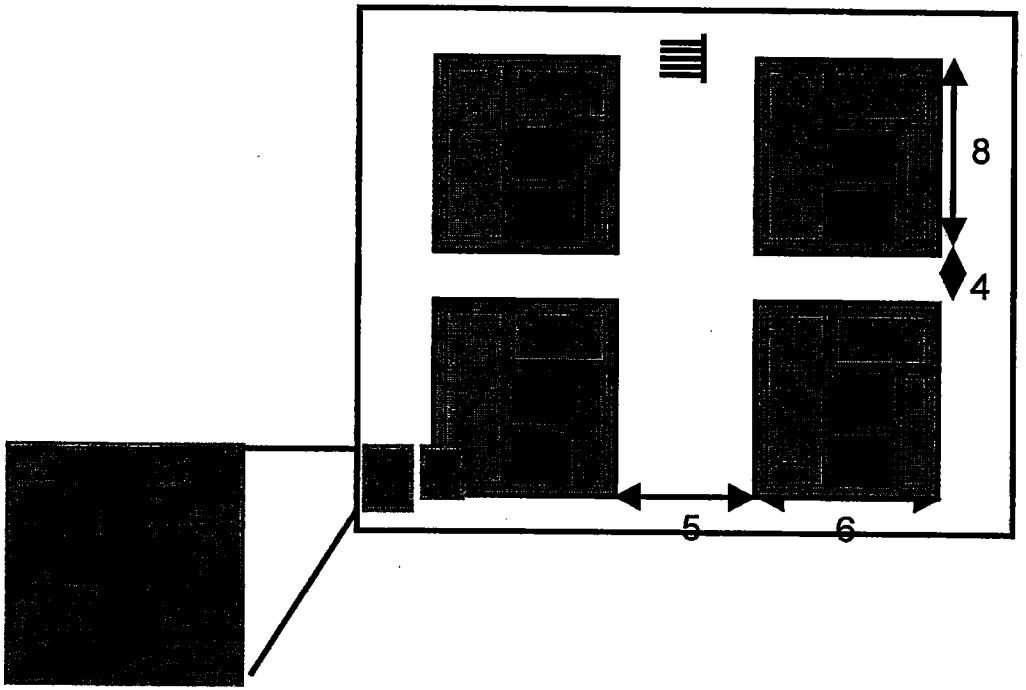

Field: Die size, Die gap, Sub products
Product 2
Product 2

| Main Applications | Motivation | Example |
|---|---|---|
| Automation | Increase tools utilization<br>Simplify the life of Yield Engineers | Transfer info of:<br>Die sizes<br>Alignment targets |
| Recipe Optimization | Increase tools performance | Care area for inspection<br>Floor plan based sampling |
| Proactive process control | focus on "yield sensitive areas" | Matched transistors<br>Dense Vs. Isolated structures<br>OPC |

**Mask information:**

- ❑ Dies sizes (length, width)
- ❑ Alignment targets (Litho Align, die corner)

- ❑ Automation
- ❑ shorten recipe generation

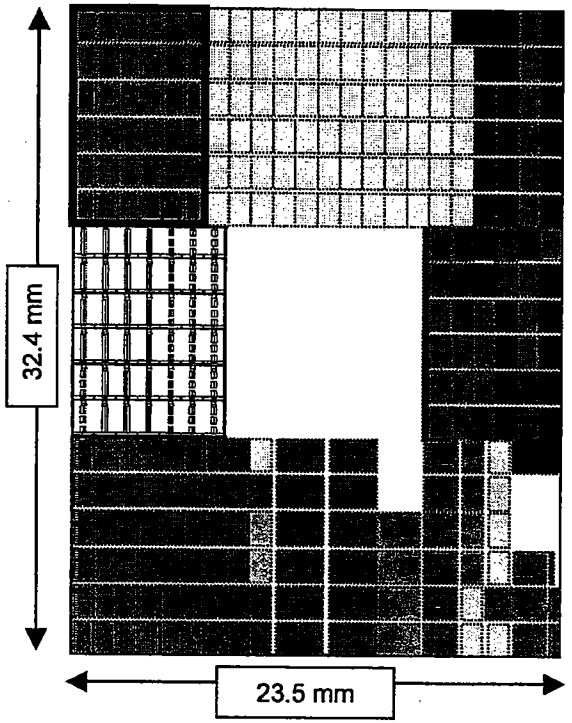


## Regions information

- Floor plan
- Periodicity

- Inspection:Auto program Care area
- Inspection: More sensitive recipe
- Sampling according to floor plan

**Die**



## Sight information

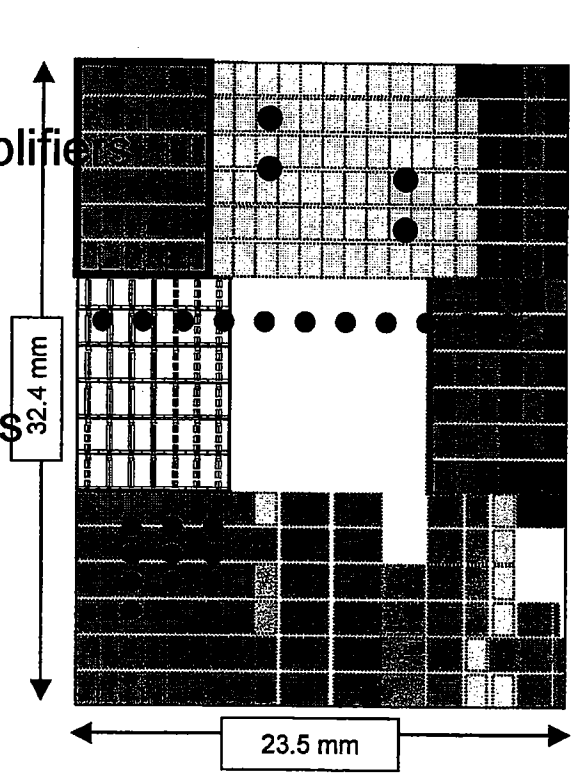
Performance-based,

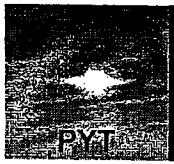
- ❑ Matched transistors in differential amplifiers

Manufacturing-base

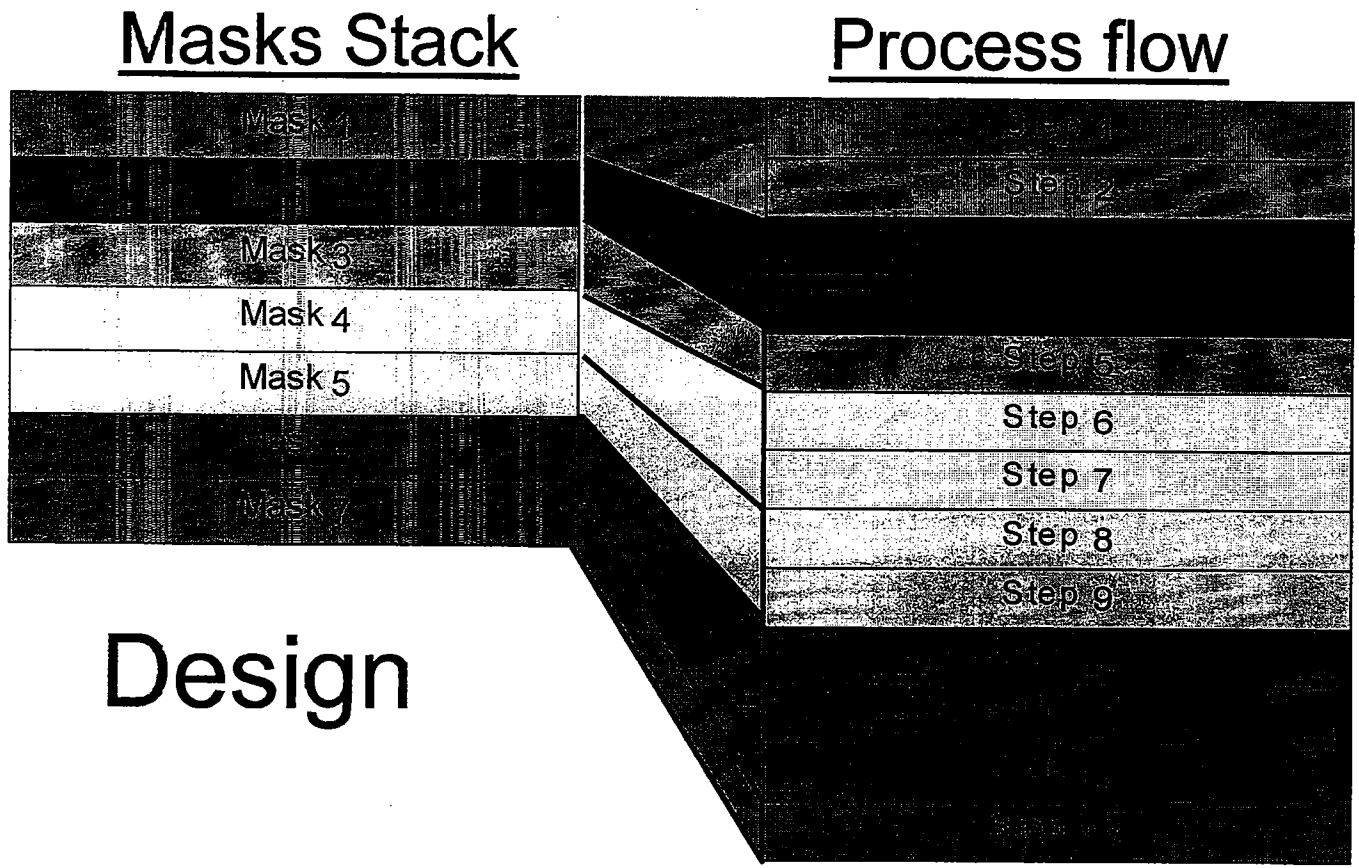
- ❑ Dense / Isolated structures
- ❑ OPC on dense versus isolated regions

- ❑ Focus on "yield sensitive sites"
- ❑ Shorten recipe generation

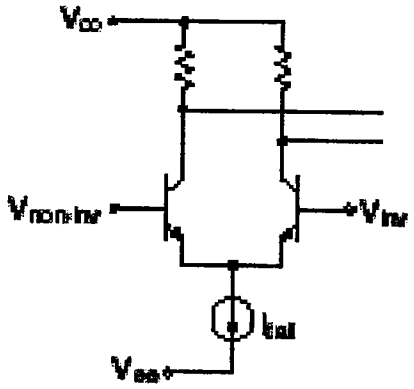


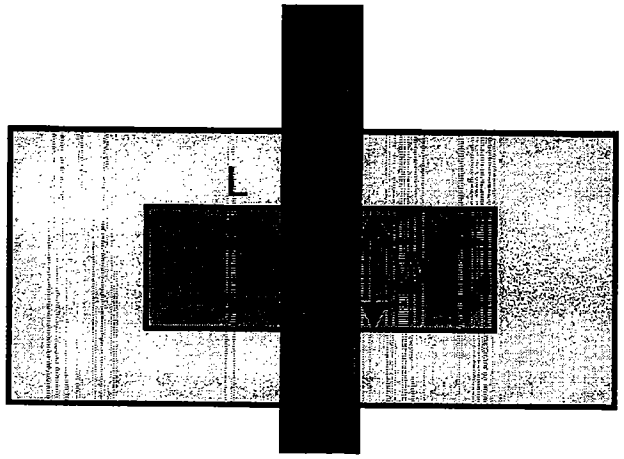


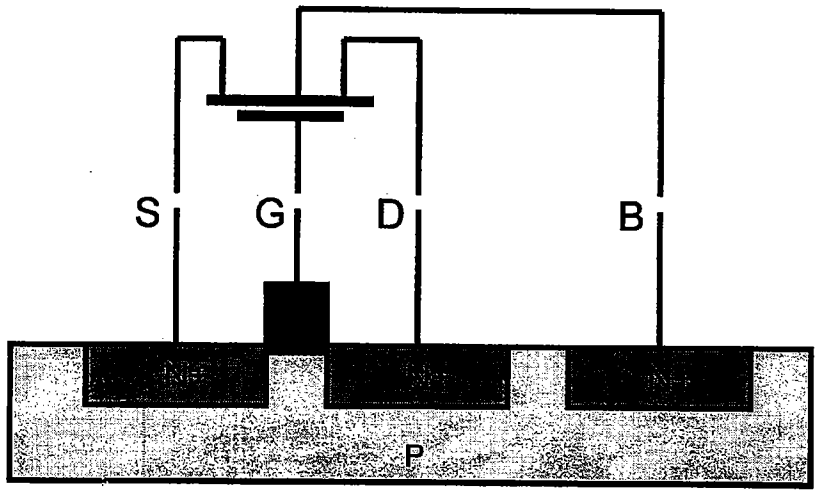

# End

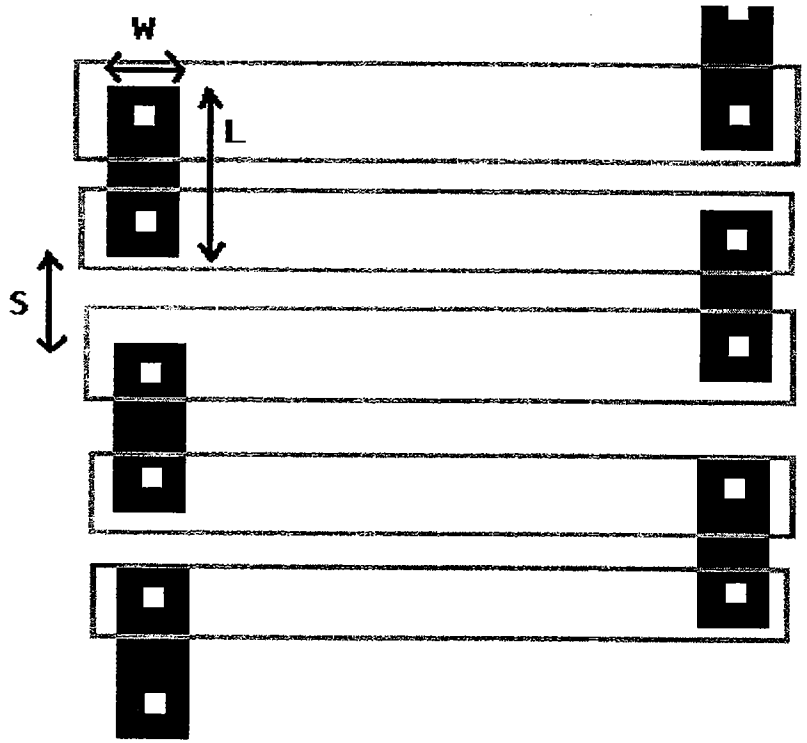

Masks Stack
Process flow
Mask 1
Mask 3
Mask 4
Mask 5
Mask 7
Step 2
Step 5
Step 6
Step 7
Step 8
Step 9
Design
Fab

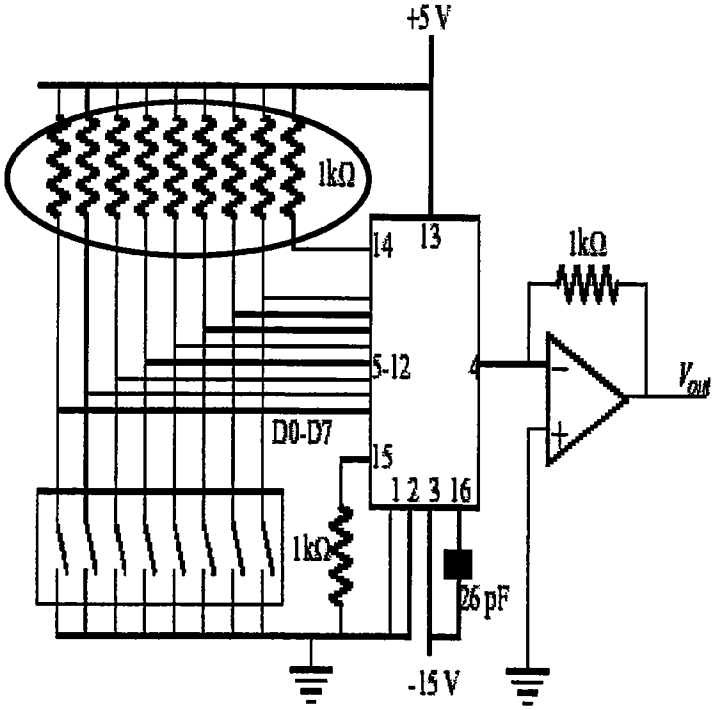
- Operational Amplifier
  - Matched transistors
    - CD measurements W, L

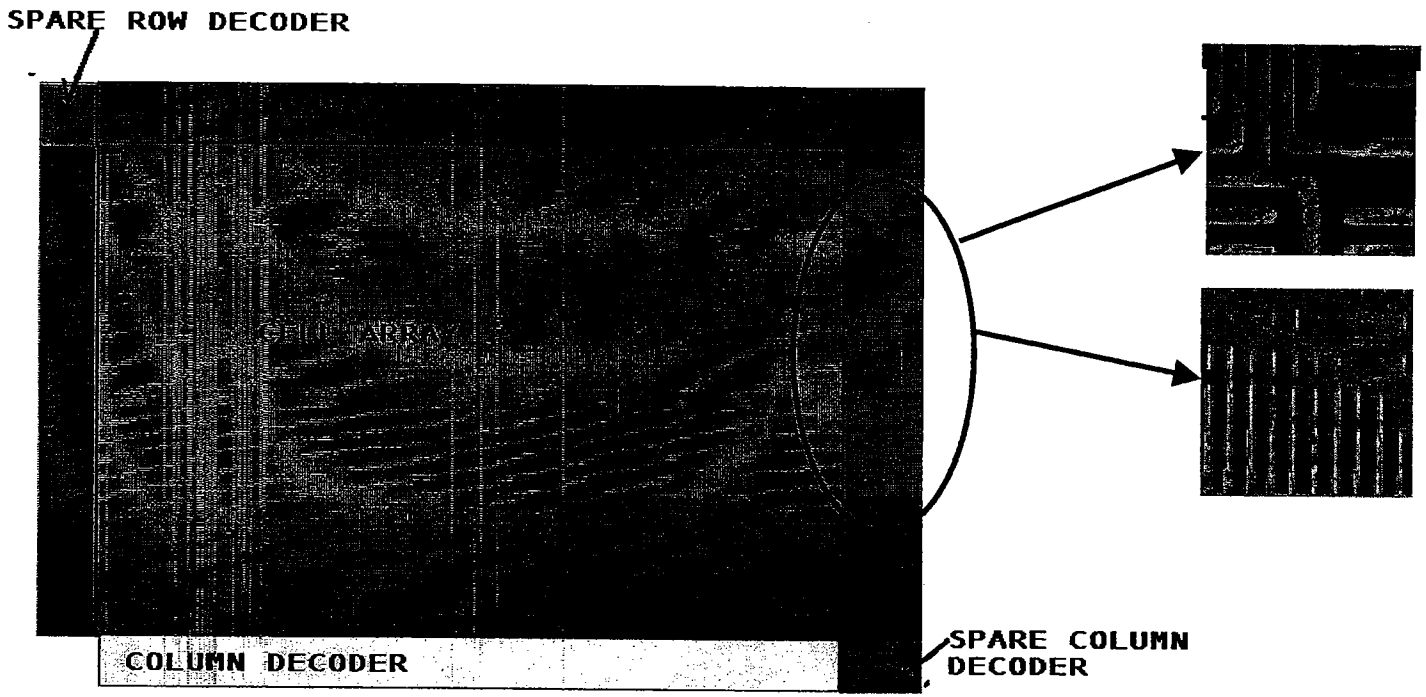



W
L
S


+5 V
1kΩ
14
13
1kΩ
5-12
4
$V_{out}$
D0-D7
15
1 2 3 16
1kΩ
26 pF
-15 V

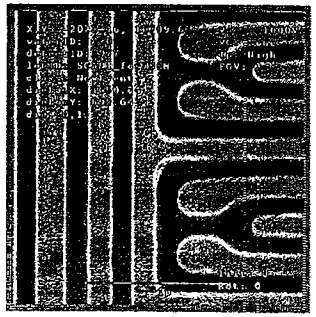


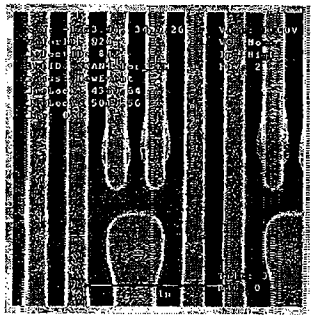

**Defect in redundancy circuitry limits repair efficiency and hence yield.**

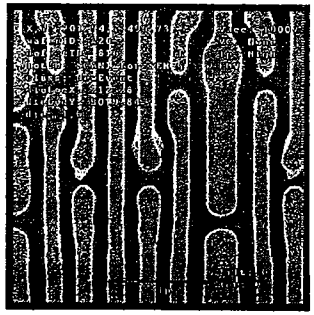
**Unrepairable die should be filtered out earlier in process to reduce production costs for memory chips.**

- Performance-based,
  - Matched transistors in differential amplifiers
  - Critical path drive transistors (clock, Bus)
  - Critical analog structures (Capacitors, resistors, NFET/PFET)
  - Non-redundant regions in memory
- Manufacturing-base
  - Dense / Isolated structures
  - Critical alignment structures (Example self alignment contacts)
  - High-MEEF locations
  - OPC on dense versus isolated regions

P.Y.T.







Systematic nal
Process & Design Interaction

**Task**

Setting up inline inspection & metrology recipes to detect process drifts (current applications on SEMVision & NanoSEM)

**Challenges**

- Current high resolution / sensitive tool sets are under utilized as customer has limited access to design data (time to information)

**Possible Solution**

- Transfer data on "yield sensitive areas" based on a set of design rules and styles

- Enables Intel
- Allows for transition from Reactive to

PDC Process Diagnostics & Control

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APPLIED MATERIALS®

Expedite

APPLIED MATERIALS®

# Design-Based Process Monitoring

## EDA to Process Monitoring Data Transfer

### Architecture Overview & Request for Comments

# Table of Contents

# 1 General

## 1.1 Preface

Applied Materials' Process Diagnostics and Control Product Group is developing a software application that will allow Metrology, Inspection and Process Monitoring machines to access information from IC design tools. This document provides an overview of a **Software Interface Architecture** that will facilitate the transfer of data from EDA software tools to Applied's Expedite System, acting as a mediator and dispatcher for in-line monitoring at the fab.
This document is provided for general guidance and as a request for comments.

## 1.2 Terms and abbreviations

| | |
|---|---|
| ADR | - Automatic Defect Review |
| API | - Automatic Process Inspection |
| CAD | - Computer Aided Design |
| EDA | - Electronic Design Automation |
| FOV | - Field Of View |
| LL | - Lower Left |
| LR | - Lower Right |
| UR | - Upper Right |
| UL | - Upper Left |

## 1.3 Revision History

| *Version* | *Date* | *Description* |
|---|---|---|
| 1 | [redacted] | Youval Nehmadi |
| 2 | [redacted] | Youval Nehmadi, Ariel Ben-Porath |

# 2 Introduction

## 2.1 Background & Motivation

In a silicon fabrication facility ("fab"), each blank silicon wafer undergoes hundreds of processing steps, among them the photolithographic printing of each layer using reticles (or "masks") as templates. Wafer processing machines ("process tools") perform the various processes, such as deposition, lithography, etching and chemical-mechanical-polishing (CMP). In addition to process tools, a wide array of metrology, inspection and review machines ("metrology tools") are utilized to continuously monitor the processes, detect out-of-control conditions and optimize yields. Various control loops are built around metrology tools in order to maintain productivity and guarantee profitability. The investment of capital and resources for process monitoring is significant in any fab, and growing rapidly with newer processes and smaller design rules, such as current 90nm Copper interconnect ICs.

In the design of integrated circuits, a multitude of software tools are employed for design and verification at various stages, from system through circuit to physical layout. At the very end of the design phase, the integrated circuit exists as a set of instructions for the fabrication of a set of reticles. These reticles, in turn, will be used in the manufacturing of the silicon wafers containing the IC.

The interface between IC design and IC manufacturing has received much attention in recent years. The software interface described below addresses one particular aspect of that interface – the optimization of process monitoring and metrology according to the product design, physical layout and functional specifications.

# 3 Architecture

## 3.1 Definitions

***Reticle-Set*** – The specific set of reticles used for the production of a wafer. A reticle set is defined as the set of ***Mask 0*** to ***Mask N***, where ***Mask 0*** is the first to be transferred to the wafer, and ***Mask N*** is the last.

***Product*** – The product is defined as synonym to a reticle-set. This is a fab's definition of a product, since it defines the actual output of the manufacturing process. Note that a product defined this way typically contains several instances of the same IC, and may even contain different ICs. Also, the product typically contains structures not associated with the IC, alignment targets and blank areas for dicing (scribe lines).

***Field, Mask-Set*** – These are also synonyms to Reticle-Set.

***Mask*** – A single mask, corresponding to a single patterning step.

***Reticle*** – Synonym to Mask.

***Die*** – A single integrated circuit, appearing once or more on the product. The data structure associated with a die encapsulates the diagnostic information related to that particular IC. Typically, a product will contain several instances of a die. In the case of a shared reticle, the product will contain several dies, each appearing one or more times.

***Non-Die*** – An area containing structures that lie outside any die in a product. The data associated with a non-die is identical to the data associated with a die, and the definition is provided to facilitate the separation between actual functional ICs and various added structures between the dies (in the "scribe lines").

***Target*** – A specific structure in a mask that is designed for aligning coordinate systems in various processing steps

***Special Structure*** – A structure located on a die or on a non-die that is designed for a specific purpose during manufacturing, such as electrically testable structures, exposure-focus matrices etc.

***Region*** – A set of rectangles within the die (or non-die) that share some characteristics as outlined in this document.

***Site*** – A set of point locations on a particular Mask that are designated by the designer or EDA tool for a specific measurement during production (e.g. measurement of critical dimensions).

***Metrology*** – We use the term metrology as a general acronym for various process monitoring and measurement activities. Examples are: critical dimension metrology, thickness metrology, optical defect inspection, electron beam wafer inspection, defect review, etch slope monitoring, and more.

## 3.2 General Requirements

1) The architecture will enable the aggregation of all data items related to a particular product in a single data structure that can be transferred to the fab by electronic, magnetic or electro-optic media. We call this structure the ***Product Diagnostic Profile (PDP).***
2) The data structure will be based on XML, to facilitate portability and enhance the ease of interfacing

3) The architecture will allow different EDA tools, used in the process of designing a single product, to append information to the PDP. The architecture will define the required synchronization (e.g. usage of a single coordinate system), the allowed discrepancies, and will recommend conflict-resolution guidelines.

4) The PDP will support shared-reticles, i.e. reticles containing different dies. Moreover, the PDP will support distributed design, so that different dies may be designed by different groups & tools, and combined into the reticle by yet another group. To support this, the PDP will possess a hierarchical structure.

5) The PDP will contain information that is directly applicable to process metrology tools for a variety of existing and potential applications

6) The PDP will provide user customization for sub-types of data items.

***Discussion:***

The general requirements above are driven by a vision in which information that is applicable to product monitoring, is incrementally extracted from different EDA tools, and appended to a single data structure. If multiple dies are combined into a single product (a shared reticle-set), the structures are combined. Eventually, the result is a single data structure, encoded on some media, which is attached to the set of reticles that are delivered to the fab for fabrication. The approach is to minimize centralization and the need for different EDA tools to communicate with each other. Each tool can append to the data structure at any time, until the data is transferred to the fab. Some global agreement between EDA tools is required, for example on coordinate systems and the transformation linking them to each other.

## 3.3 Overall architecture

The data structure is organized in a straightforward hierarchy that reflects the organization of a product into dies and non-dies, and the organization of each of those into mask levels. Beyond the masks, the data is organized into four categories that are derived from a process metrology view of the product. These categories are ***Targets***, ***Special Structures***, ***Regions*** and ***Sites***. The motivation and guidelines for this partition are as follows:

***Targets*** – These are structures used for precise alignment of wafers in metrology tools (as well as other process tools, such as steppers and scanners). They are not related to a particular metrology application.

***Special Structures*** – These are structures, typically (but not necessarily) in non-dies, that are inserted for specific functions related to the manufacturing process. Examples are electrically or otherwise probe-able test structures, focus-exposure matrices, CMP characterization test structures, OPC characterization structures.

***Regions*** – These are relatively large die (or non-die) areas that share some geometrical or functional qualities that can be utilized by metrology tools to optimize productivity, sensitivity, throughput or quality of information.

***Sites*** – These are specific locations (i.e. X,Y coordinates) where specific measurements and/or requirements are made by the designers. They can reflect functional, manufacturability or other aspects, and provide designers with a direct link to process monitoring, allowing them to specify what are the critical locations for measurement and the acceptable tolerances.

***Figure 1*** is a graphical overview of the architecture. Note that the structure of a die and non-die is identical, and the distinction between them is for clarity only. As described above, a product typically has multiple instances of a die. These instances will be specified in fields contained with the product, and are not related to the multiple dies showing in the figure. The multiple dies showing in the figure (namely, die 2 to die n) will only exist in a shared reticle-set, where multiple ICs are manufactured on the same product.

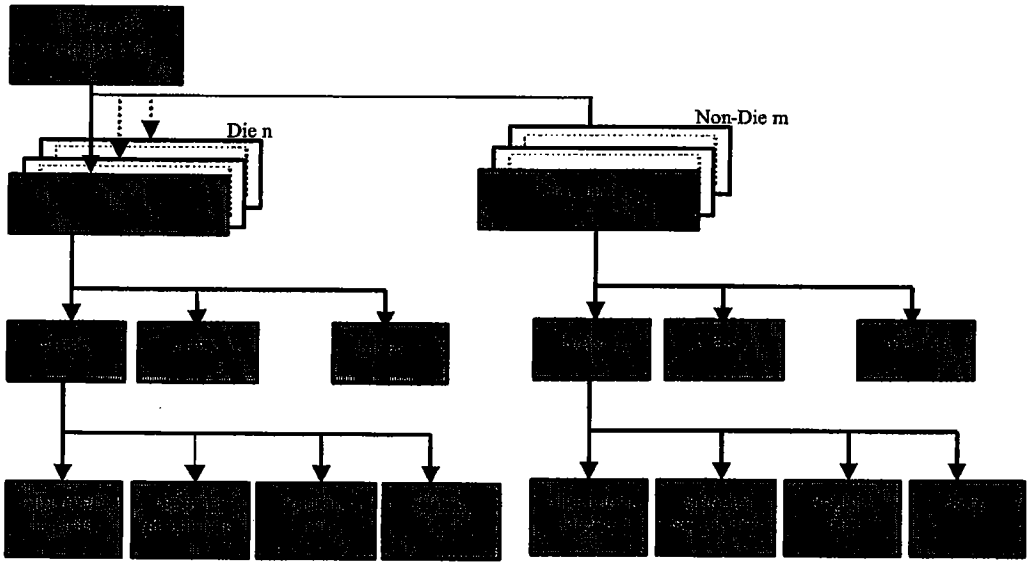


**Figure 1 – Schematic View of the Product Diagnostic Profile (PDP) data structure. See text for details.**

## 3.4 Coordinate systems

### 3.4.1 Space & Type

All coordinates are in a two-dimensional space and specified using Cartesian X,Y pairs. There is no three-dimensional information embedded in coordinates.

### 3.4.2 Units

All coordinates are measured in ***Microns*** (*μM*), and expressed as floating numbers. Wherever possible, resolution of ***0.1 nM*** (*=0.0001 μM*) should be provided.

### 3.4.3 Frames of Reference

A single ***Product Diagnostic Profile*** contains the following frames of reference:

1. ***Product Coordinates*** – This is "parent" frame of reference, expressing physical coordinates on the reticle set. Each PDP defines a single product coordinate system, as further described below.
2. ***Die Coordinates*** – For each die (or non-die) object, all location data must be expressed in a single coordinate system, called ***Die Coordinates***.

Coordinate Transformations:

1. Each Product will contain a transformation matrix **D** for each of its daughter dies and non-dies that will specify a rotation and/or mirroring transformation. In addition, each product will also contain an offset vector for each instance of each daughter die and non-die, that will provide the location of the origin of die coordinates for the particular instance. Taken together:

$$\begin{bmatrix} Xp \\ Yp \end{bmatrix} = D \begin{bmatrix} Xd \\ Yd \end{bmatrix} + \begin{bmatrix} Xo \\ Yo \end{bmatrix}$$

Where ***Xp,Yp*** are product coordinates, ***D*** is a 2-by-2 matrix **associated with the die,** whose elements are {0,-1,+1}, ***Xo*** and ***Yo*** are non-negative values giving the location of the origin and **associated with a particular instance of the die**, and ***Xd, Yd*** are die coordinates.

The Product Coordinate system must be a lower-left coordinate system, with the X axis increasing to the right, and the Y axis increasing to the top. Negative Product Coordinates are therefore illegal. Die coordinate systems can have an arbitrary orientation, but must all lie in the first quadrant of that system, i.e. only non-negative values of X,Y are allowed.

**Note 1:** Product Coordinates are applicable to all mask levels. Special care should be noted when a specific mask has a unique mask-to-wafer reduction ratio associated with it.

**Note 2:** The limitation on elements of D being {0,-1,+1} implies that die coordinates can only be rotated in increments of 90 degrees, and/or mirrored. In other words, dies cannot be placed "diagonally" on products.

**Note 3:** A product contains a matrix ***D*** for each daughter die, however it contains an offset vector ***Xo,Yo*** for each instance of each die.

### 3.5 Images

The architecture allows the transfer of graphical descriptions of small patches of the layout, namely targets and sites. We refer to these as "images", and provide a very broad definition. Some of the applications will be using the images for visual reference only, as part of an interactive application, while others may perform automated image analysis and processing.

- Images are used in targets and sites.
- The maximum field of view for an image is 50 Micron in each axis.
- The target/site should be located in the center of the FOV, whenever possible
- The allowed image format will include standard graphics formats (TIFF, JPEG, BMP etc.), GDS II and MEBES.
- The image will described by the following attributes: Image File Reference, Image Lower Left Corner die coordinates, Image Width & Height.

## 4 Format

Data will be transferred from EDA tools into Applied's Expedite application running on the production floor via a file-based interface. The set of files accompanying a reticle set entering the fab is referred to as the Product Diagnostic Profile (PDP).

A major requirement is to enable different EDA tools to generate different parts of the PDP, for example: An OPC tool may output sites for OPC metrology, and an electrical verification tool may output site for matched transistor metrology. The format must therefore enable appending to an existing PDP in a flexible manner. On the other hand, all writers to the PDP must share some global variables describing the field geometry. To accommodate these requirements, the implementation will include two XML schemes:

- Product Scheme - An object that will define the coordinate system, the mask set and the mapping of different dies to the field. There will be a single instance (i.e. single XML file) of this scheme, and its generation must be coordinated between the various EDA tools
- Die Scheme – An object that will define all the remaining information, as described in this document. Multiple instances (i.e. multiple XML files) may exist, and the information from each will be appended by Applied's Expedite Application.

# 5 Data Objects

## 5.1 Image

Images are optional for sites and targets, as described in section 3.5. Each image is represented by the following structure:

`ImageInformation`

- **`ImageFileReference`** – A reference that allows selection of the appropriate image file
- **`ImageLowerLeftX, ImageLowerLeftY`** – Die coordinates of the image lower left corner
- **`ImageSizeX, ImageSizeY`** – Width and Height of the image

## 5.2 Product

The product typically contains several instances of the same IC, and may even contain different ICs. Also, the product typically contains structures not associated with any IC, such as alignment targets and blank areas for dicing (scribe lines). We refer to each unique IC design as a ***Die***, and unique grouping of other features as a ***Non-Die***. The product typically has ***multiple instances*** of each die and non-die The Product structure will contain the following fields:

- **`FieldSizeX, FieldSizeY`** - The size of the field
- **`MaskTable`** – A table that contains the set of all masks used in the process. Each entry in the table contains:
  - **`MaskIndex`** - Starting from Mask 0, the first mask in the process
  - **`MaskName`** – A descriptive name for the mask
- **`DieTable`** - A table that will specify for each die the following information (see Table 1 and Figure 2):
  - **`DieID`** – A unique integer identifier to the die. The set of all dies and non-dies must not have duplicates of this identifier.
  - **`DieName`** – An arbitrary string containing the name of the integrated circuit (or some other descriptive name, in case of a non-die).
  - **`DieOrNonDie`** – Two-value Flag to indicate a die (actual IC) or non-die (some grouping of auxiliary structures.
  - **`DieCoordinatesConversionMatrix`** – The coordinate conversion matrix ***D***, as described in section 3.4.

- `DieInstanceList` – A list of 4 values for each instance of the die (or non-die):
  - `DieOriginX0, DieOriginY0` – Location of the die coordinates origin, corresponding to the values ***X0, Y0*** from section 3.4.
  - `DieSizeX, DieSizeY` – Size of the die. This is used for clipping all die coordinates to lie within the resulting rectangle.

| FieldSizeX = 43400<br>FieldSizeY = 33300 | | | | |
|---|---|---|---|---|
| Die ID | Die Name | Die / Not Die | Die Coor. Convert Matrix | DieInstanceList (DieOriginX0,DieOriginY0,DieSizeX, DieSizeY) |
| 1998 | Mem GB500 | Die | $\begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}$ | (100,100,18000,16500), (20000,100,18000,16500), (100,16700,18000,16500),(20000,16700,18000,16500) |
| 5112 | TectICXY | Die | $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ | (36300,100,7000,16500), (36300,16700,7000,16500), |
| 31 | Align Targets | Not Die | $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ | (18125,100,50,8000), (18125,18200,50,8000) |

**Table 1 – Example of a product containing two ICs and one non-die.** In this example, the field contains four instances of one IC, two instances of a second IC and two instances of a target area located within the scribe-line. Note that no assumptions are made on regularity of the field, and in this example the field is rectangular rather than square, and the vertical scribe-lines are not evenly spaced.

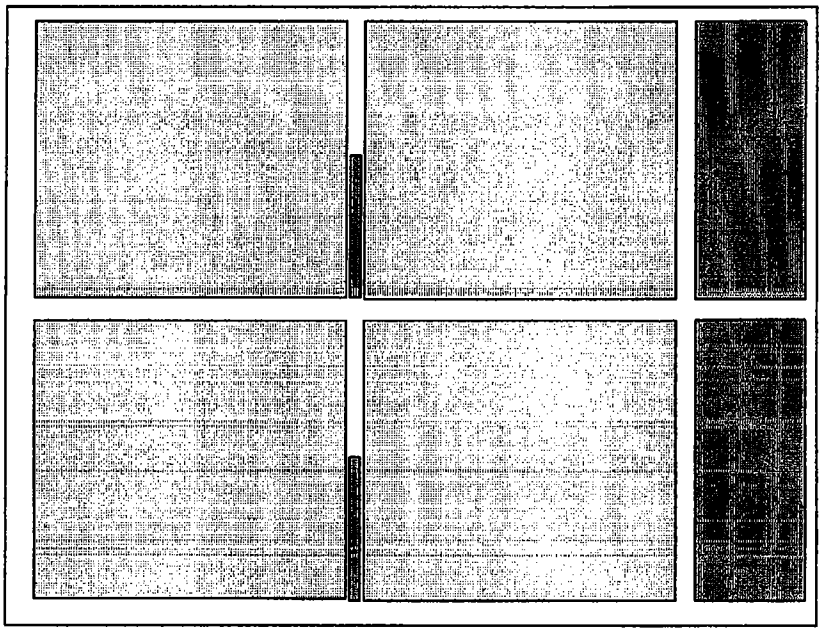

**Figure 2 - A graphic representation of the field depicted in the example in Table 1.** Each shading pattern represents a different die, showing four instances of one IC, two instances of a second IC, and two instances of a scribe line test area. The drawing is not to scale, in order to enable visualization of the scribe lines.

### 5.3 Die (and Non-Die)

The die (or non-die) attributes are contained in the parent product object. The die object does not contain any additional attributes.

### 5.4 Mask

The Mask objects contains two attributes: **`MaskIndex`**, **`MaskName`**. They must match an existing entry in **`MaskTable`**, see section 5.1.

### 5.5 Alignment Target

Alignment targets are targets that are needed to align various process and metrology tools that are location dependent (e.g. stepper/scanner, defect inspection). The information provided by the alignment targets will be the following (see **Error! Reference source not found.**):

- **`TargetType`** - Allowed Types are
  - Stepper
  - Overlay
  - Corner LL
  - Corner UL
  - Corner UR
  - Corner LR
  - User defined
- **`TargetName`** – A string containing a descriptive name
- **`TargetLocationX`**, **`TargetLocationY`** – Coordinates of the target. Should be close to the center of a tightly bounding rectangle.
- **`TargeImageInformation`** (Optional) – An **`ImageInformation`** structure

### 5.6 Special structures

TBD

## 5.7 Regions

The Region object provides information derived from multiple segmentations of the die. Each ***Segmentation Scheme*** is based on a single geometrical or functional property, and results in a list of sections, as described below. For example, one segmentation scheme is according to the pitch of the region, and another segmentation scheme is according to the redundancy built into the region. Each segmentation scheme results in a list of ***Sections***.
The set of segmentation schemes is given in Figure 3.

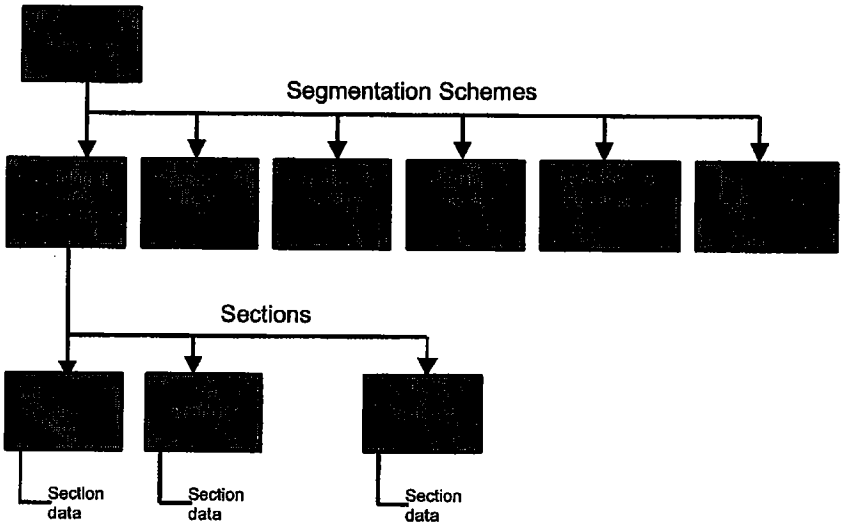


**Figure 3 - Segmentation Schemes**

### 5.7.1 Description

Each Section in the Segmentation Scheme will have its own Section data according to the Section's characteristics. The Sections within the same Segmentation Scheme are mutually exclusive (not overlapping) zones that cover part or all of the die (or non-die). Each Section is a unification of mutually exclusive (not overlapping) rectangles, sharing the same value for the selection criterion of the parent Segmentation Scheme (see example in Figure 4).

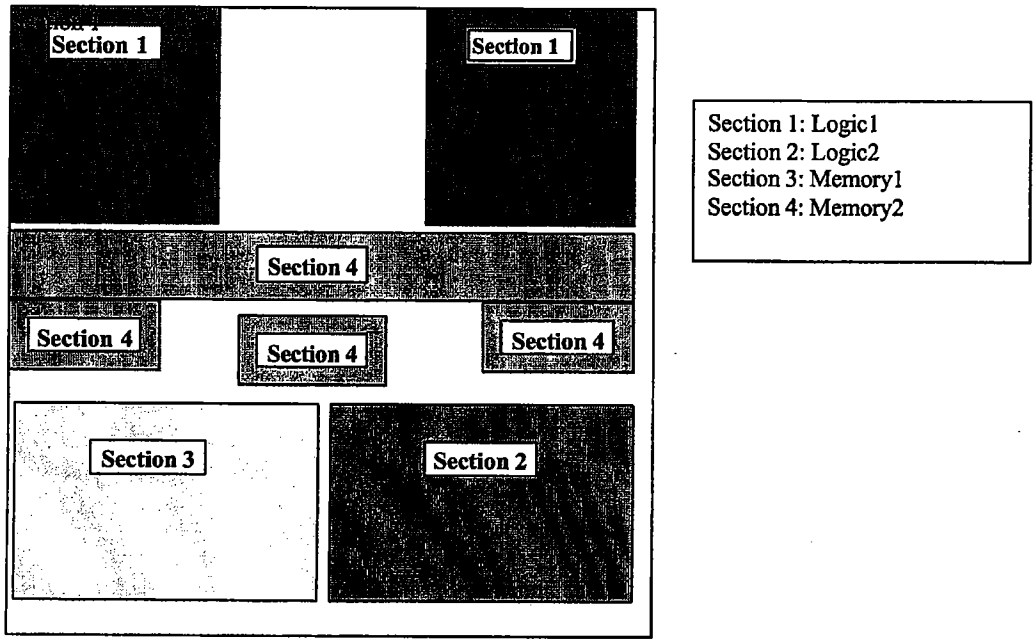


**Figure 4 - Example for segmentation of a die according to Segmentation Scheme 3 – Function** The values for the ***Function*** attribute are user-defined. Section 1 is the union of rectangles defined to have Function "Logic 1", and Sections 2-4 are defined similarly.

Each Section data structure contains data related to the Section's Segmentation Scheme. A single structure will be used for all sections. However, each Segmentation Scheme will be associated with a subset of mandatory fields, as specified in Table 2, and other fields are optional.

- **`RectangleList`** – This is a list of rectangles that describes the zones belonging to the specific Section.
- **`Function`** The device functionality (Cell Array, Column Decoder, Row Decoder, Redundancy Circuit, Logic, JTEG, Unknown, etc.).
- **`ExactPeriodicity`**
    - Major Period

  - Major Orientation as measured in lower-left coordinate system from X axis.
  - Minor Period (comment: Minor orientation is perpendicular to major orientation)
- **GeometryType** - (Lines vertical, Lines horizontal, Lines Manhattan, Lines X, holes, islands, etc.).
- **Random** (No = good for cell to cell).
- **Redundancy** – The minimum number of defected features that will kill the die (especially in memory cell).
- **PitchDistribution**
  - **PatternWidthDistributionX** – The vector that will specify the probability for each pattern width.
  - **PatternWidthDistributionY** – The vector that will specify the probability for each pattern width.
  - **SpaceWidthDistributionX** – The vector that will specify the probability for each space width.
  - **SpaceWidthDistributionY** – The vector that will specify the probability for each space width.
  - **PeriodDistributionX**– The vector that will specify the probability for each period width.
  - **PeriodDistributionY**– The vector that will specify the probability for each period width.
- **UserComment** - String

**Note 1:** The number of Sections under a single parent Segmentation Scheme cannot exceed 50.
**Note 2:** The size of any single section will be at least 2500 $\mu^2$M.

| Field | Segmentation types | | | | | |
|---|---|---|---|---|---|---|
| | Exact period | Pitch | Criticality | Function | Redundancy | User defined |
| Rectangle List | X | X | X | X | X | X |
| Device function | | | | X | | |
| Section periodicity | X | | | | | |
| Geometrical type | X | X | | | | |
| Random | | | | | | |
| Redundancy | | | | | X | |
| Analysis orientation | | | | | | |
| Pattern/Space/Period distribution | X | X | | | | |
| User Comment | | | | | | |

**Table 2 - Mandatory fields for the different Segmentation Schemes.** Note that the only data mandatory for all segmentation types is ***Rectangle List***.

### 5.7.2 Exact Period

In an exact period section all the structures are repetitive with this spatial period (starting from each location in this section if we move in steps of the period we will be exactly at the same structure). High resolution images (e.g. SEM images) taken on the wafer at multiples of the period can be overlaid for an exact match. The section period is the smallest period that can represent it. If the section contains multiple rectangles, they all share the same period and a single identical repeating structure. An alternative formalization of this requirement is that a single patch of image can be used as a "golden" reference for comparison with any patch of the section.

The most important sections are sections with periods in the of range 2 to 40 microns (μM).

### 5.7.3 Pitch

Pitch sections are defined by characteristic period in their spatial structure. Unlike Exact Period Sections (see 5.7.2), they do not contain exact replicas of a basic structure, and may have extensive variability in the design.
Details are TBD.

### 5.7.4 Function

A section will be defined according to its functionality, as extracted from the die floor plan. A master list of functions is TBD, which will include such entries as:

- SRAM Array
- DRAM Array
- Flash Array
- Column Decoder
- Row Decoder
- Redundancy Circuit

- Logic
- JTEG
- Line Drivers
- Parallel Bus
- Analog Amp
- RF Amp
- User Defined String

### 5.7.5 Criticality

This segmentation scheme will be related to the sensitivity of the section to defects. Generally, a section will have higher criticality if it is more susceptible to malfunction due to defects, for a given defect size range. Exact definition is TBD.

### 5.7.6 Redundancy

A section with redundancy N is defined as section where at least N features must be defective in order to induce a possible die failure. This relates to memory cell sections with built-in redundancy, as well as other redundant circuits.

### 5.7.7 User-Defined

A string containing a user defined function.

## 5.8 Sites

Sites are specific locations (i.e. X,Y coordinates) where specific measurements and/or requirements are made by the designers. They can reflect functional, manufacturability or other aspects, and provide designers with a direct link to process monitoring, allowing them to specify what are the critical locations for measurement and the acceptable tolerances. A single Site is defined as a set of point locations, each with an optional image, and a single set of metrology attributes for all locations.

### 5.8.1 Site General Information

Each Site structure contains the following information:

- **`SiteTable`** - A table that describes the pre-defined locations for measurements and inspection. The sites may be divided into pre-defined groups. Each group is a set of devices that should match each other (e.g. matched transistors). The collection of the locations of these devices will be placed in the same column (**`CompareNum`**). The different recurrences of the same device on the same die are grouped in the raw (**`LocationNum`**) (see Table 3).
- **`DeviceType`** - The type of the feature that should be monitored. A device type can be one of the following:
  - Gate

- Conductor
- Assist
- User Defined

- **`MonitorType`** – The monitoring method that will be applied on the device:
  - Process Inspection
  - Width
  - Diameter
  - Minimum Distance (between devices)
  - Maximum Distance (between devices)
  - 3D Profile
  - Matched width
- **`MonitoringSpec`** – It describes the required specification for the measurement. The MonitoringSpec will have the following fields:
  - Min - The minimum accepted
  - Max - The maximum accepted
  - Std Dev - The accepted Std Dev
- **`MonitoringMotivation`** – The motivation for monitoring this device. It can have the following values:
  - Circuit Critical Timing
  - Circuit Matched Transistors
  - Circuit Matched Resistors
  - Marginal to Design Rule
  - Dense Layout
  - Isolated Feature
  - OPC issue
  - High MEEF
  - Process Dishing & Erosion
  - Process Step Coverage
  - User Defined
- **`MeasurementSpec`**
  - Direction - The required measurement direction
  - Measurement Comment – user-defined string

- **`AdditionalInfo`** – User-defined string.

| | Location 1 | Location 2 | Location 3 | Location 4 |
|---|---|---|---|---|
| Compare 1 | x,y | x,y | x,y | x,y |
| Compare 2 | x,y | x,y | x,y | x,y |
| Compare 3 | x,y | x,y | x,y | x,y |
| Compare 4 | x,y | x,y | x,y | x,y |

**Table 3 Site Squares Table example**

### 5.8.2 Site Images

- **`TargeImageInformation`** (Optional) – An **`ImageInformation`** structure that describes the device that needs to be monitored.
- **`LocationID`** – A combination of **`(CompareNum, LocationNum)`.**
- **`ImageList`** - Each Image will have the relevant **`LocationID`**.

| Image Number | FOV (Micron) | Location IDs (Compare Num, Location Num) |
|---|---|---|
| Site image 1 | 50 | (1,1), (3,3), (3,2) |
| Site image 2 | 40 | (1,2), (3,2), (3,2) |
| Site image 3 | 40 | (1,3), (3,1), |

**Table 4 Site Image information**

# 6 Format

Data will be transferred from EDA tools into Applied's Expedite application running on the production floor via a file-based interface. The set of files accompanying a reticle set entering the fab is referred to as the Product Diagnostic Profile (PDP).

A major requirement is to enable different EDA tools to generate different parts of the PDP, for example: An OPC tool may output sites for OPC metrology, and an electrical verification tool may output site for matched transistor metrology. The format must therefore enable appending to an existing PDP in a flexible manner. On the other hand, all writers to the PDP must share some global variables describing the field geometry. To accommodate these requirements, the implementation will include two XML schemes:

- Product Scheme - An object that will define the coordinate system, the mask set and the mapping of different dies to the field. There will be a single instance (i.e. single XML file) of this scheme, and its generation must be coordinated between the various EDA tools

- Die Scheme – An object that will define all the remaining information, as described in this document. Multiple instances (i.e. multiple XML files) may exist, and the information from each will be appended by Applied's Expedite Application.

# 7 Appendix A – Fab configuration

The Fab configuration contains additional information that will be provided to the Expedite Application externally, and not via the EDA information. This will include:

- **`MaskMagnification`** The magnification of the mask
- **`StepperStepsX`**, **`StepperStepsY`** – The stepper steps in X and Y directions.
- **`WaferCenter2FieldOffsetX`**, **`WaferCenter2FieldOffsetY`**– The location of the first field relatively to the wafer center.